INSTRUCTIONS

GEK-45476A

SUPERSEDES GEK-45476

STATIC

NEGATIVE SEQUENCE

OVERCURRENT RELAY

TYPE SLCN51D

GENERAL ELECTRIC

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STATIC NEGATIVE SEQUENCE OVERCURRENT

TYPE SLCN51D

DESCRIPTION

The SLCN51D is a solid-state negative-sequence directional-overcurrent relay for directional comparison protection of transmission lines. The relay is packaged in one 4-rack unit high case suitable for standard 19-inch rack mounting. The relay outline and mounting dimensions are shown in Figure 2.

The SLCN51D includes forward and reverse blocking negative-sequence directional functions designed to respond to all types of unbalanced faults. Various negative, positive, and zero sequence overcurrent functions are also included for fault detection and supervision of other measuring functions utilized in * the directional-comparison pilot-protection schemes. The SLCN51D is normally applied with a type SLYP positive-sequence distance relay which includes measuring functions designed to respond to balanced three-phase faults. Other equipment in a typical terminal would include a type SLA logic relay, a type SLAT output relay, and a type SSA regulated power supply. Various other measuring relays may also be included in special schemes which employ single-pole tripping.

The functions which may be included in an SLCN51D relay are as follows:

$D_2(T)$	- Tripping negative-sequence-directional function.
$D_2(B)$	- Blocking negative-sequence-directional function.
$(I_2\text{-}K\ I_1)\ (T)$	- Negative-sequence-overcurrent fault detector with positive sequence restraint.
$I_2(B)$	- Negative-sequence-overcurrent function for blocking supervision.
$I_1(T)$	- Positive-sequence-overcurrent function for trip supervision.
$I_1(B)$	- Positive-sequence-overcurrent function for blocking supervision.
$(I_0\text{-}K\ I_1)\ T$	- (OPTIONAL) Zero-sequence direct-trip overcurrent with positive sequence restraint.
$I_0(T)$	- (OPTIONAL) Sensitive zero-sequence fault detector for weak infeed or single pole tripping schemes.
$(I_0\text{-}K\ I_1)\ (T)$	- (OPTIONAL) Zero-sequence supervising fault detector with positive-sequence restraint for single pole tripping schemes.
I_1T	- (OPTIONAL) Positive-sequence direct-trip-overcurrent function.
I_2T	- (OPTIONAL) Negative-sequence direct-trip-overcurrent function.
I_2TOC	- (OPTIONAL) Negative-sequence time-overcurrent function.

The overall logic diagram and the relay nameplate indicate which of the optional functions are included in a particular equipment. All SLCN51D relays include the wiring and sockets for all the above functions. When any optional function is omitted in a particular SLCN51D this function may be subsequently added in the field by obtaining the necessary printed circuit cards and inserting them in the proper sockets. However, the addition of optional functions to an existing equipment does require that any associated circuits in other relays in the equipment be present or added at that time.

* Indicates revision

The internal connections diagram for the SLCN51D relay is shown in Figure 1, and the component location diagram is shown in Figure 3. Detailed information on the various printed circuit cards is included in GEK-34158.

APPLICATION

The SLCN51D is a negative-sequence directional-overcurrent relay which includes various other positive and zero-sequence-overcurrent functions. The relay is designed for use with a type SLYP positive-sequence-distance relay to provide complete directional comparison protection for all types of faults on transmission lines. The relay is suitable for operation on lines with series capacitor compensation, and on uncompensated lines. The relay can also be applied with single-pole-tripping schemes which employ additional measuring functions for the determination of which phases are faulted.

The basic measuring functions in the SLCN51D are the combination of $D_2(T)$ and $(I_2\text{-}K\ I_1)\ (T)$ which provide the tripping function for unbalanced faults, and the $D_2(B)$ function which provides the blocking function. The $(I_2\text{-}K\ I_1)\ (T)$ is a negative-sequence-overcurrent function with positive-sequence restraint which is used as the tripping level fault detector for unbalanced faults. This trip fault detector is supervised by the $D_2(T)$ forward-looking negative-sequence-directional unit in directional-comparison schemes. $D_2(T)$ is negative-sequence voltage polarized with supplemental negative-sequence current polarization to assure that an adequate polarizing quantity of the correct polarity is present for all types of faults and all fault locations.

The $D_2(B)$ is a similar negative-sequence-directional unit looking away from the protected line section. $D_2(B)$ provides the blocking function for external unbalanced faults behind the relay. An $I_2(B)$ negative-sequence-overcurrent function is also included for supervision of the $D_2(B)$ and $D_2(T)$ directional functions.

$I_1(T)$ and $I_1(B)$ positive-sequence-overcurrent functions are included in the SLCN51D. These level detectors are operated from the output of the positive-sequence-current network in the associated SLYP relay. The $I_1(T)$ and $I_1(B)$ are used for current supervision of the positive-sequence tripping and blocking functions, respectively, in the associated SLYP relay. This overcurrent supervision is primarily intended to prevent outputs of the positive-sequence-distance functions during the deenergizing transients of lines with shunt reactors. The $I_1(T)$ may also provide security for a condition of potential failure if the application permits the use of pickup settings above load current.

The optional $(I_0\text{-}K\ I_1)T$ zero-sequence direct-trip function provides high speed tripping on heavy single and double line-to-ground fault currents. The use of positive-sequence restraint tends to provide a larger margin between the net operating quantities on internal and external faults. The larger margin results from the normally higher ratio of zero-sequence line impedance to the positive-sequence line impedance, when compared to the ratio of the zero-sequence to positive-sequence "source" impedance at each end of the line. The positive-sequence restraint tends to be more effective on long-series-compensated lines.

An optional $I_0(T)$ sensitive zero-sequence-overcurrent level detector is available for use in special schemes designed to accommodate weak-infeed terminals which may have insufficient fault current to operate the primary directional and distance functions. This $I_0(T)$ function is also used in certain schemes for single-pole tripping to supervise the measuring functions provided to determine which phase is faulted.

An optional $(I_0\text{-}KI_1)\ (T)$ positive-sequence restrained zero-sequence-overcurrent function is also available for supervision of the positive-sequence mho tripping function in special single-pole tripping schemes to provide security against possible 3-pole tripping on single phase faults under certain conditions.

* An optional positive-sequence overcurrent function, I_1 T, is available for applications where very large fault currents for near end faults require maximum relaying speed.

* An optional negative sequence overcurrent function, I_2T, is available for the same purpose as I_1 T.

If I_2T is not used, an optional negative-sequence very-inverse-time-overcurrent function, I_2TOC, is available. I_2 TOC provides a backup function. Generally, logic circuitry is available in the SLA to provide directional supervision of I_2TOC, for those applications where directional supervision is desirable.

Refer to the applicable scheme Logic Diagram and Logic Description for the particular equipment for the specific functions included and the circuit arrangement in which they are applied, including the relationship with the pilot channel employed in the particular scheme. The proper external connections for the SLCN51D are shown on the elementary diagram furnished with the overall equipment.

* Indicates revision

RATINGS

The type SLCN51D relay is designed for use in an environment where the ambient temperature around the relay case is between -20°C and +65°C.

The type SLCN51D relay requires a ± 15 volt d-c power source which can be obtained from a type SSA50/51 power supply.

The current circuits of the type SLCN51D relay are rated for 5 amperes, 60 hertz for continuous duty and have a one-second rating of 300 amperes.

The potential circuits are rated for 120 volt a-c.

BURDENS

The type SLCN51D relay presents a maximum burden to the type SSA power supply of:

200 ma from the +15 volt d-c supply

100 ma from the -15 volt d-c supply

The burden presented by the current circuits at 5 amperes is (Later)

The burden presented by the potential circuits at 120 volt a-c is (Later)

RANGES

The ranges given in this section are typical for the type SLCN51D relay. Refer to the unit nameplate for the ranges of a particular relay.

A. Overcurrent Units

I_2(B)	0.2 - 0.6A		negative sequence
I_2T	2 - 16A		negative sequence
I_1(B)	0.5 - 4.0A		positive sequence
I_1(T)	1.0 - 8.0A		positive sequence
I_1T	4.0 - 32A		positive sequence
I_0(T)	0.3 - 2.4	$3I_0$**	
(I_2-K_1I_1)(T)	0.3 - 3.0A $0.1 \leq K_1 \leq 0.3$		negative sequence
I_2TOC	0.2 - 3.0A		negative sequence
(I_0-K_TI_1) (T)	1.0 - 3.0A $0.4 \leq K_S \leq 0.8$	$3I_0$**	
* (I_0-K_TI_1)T	2.0 - 20A $0.15 \leq K_T \leq 0.45$ (F114)	$3I_0$** or	0.3 - 3.0A $3I_0$** $0.1 \leq K_T \leq 0.3$
G_4	2.0 - 20A	$3I_0$**	

** Ranges are given for 3Ω base reach tap, for the ranges on the 1Ω tap, multiply given range by 3.

B. Directional Unit

Offset range in ohms: 0.5 - 10.0

Sensitivity:

Current: 0.2A negative sequence

Voltage: 0.25 V negative sequence (factory setting)

* Indicates revision

OPERATING PRINCIPLES

A. Introduction

The SLCN51D relay uses signals derived from the secondary currents and voltages as operating quantities for the various measuring functions included in the unit. The positive-sequence signal is supplied by a type SLYP relay. The zero and negative-sequence quantities are derived in the type SLCN51D relay.

B. Negative-sequence Voltage Network

The negative-sequence voltage network is shown on the internal connection diagram of Figure 1. The negative-sequence voltage network consists of three phase-to-phase voltage transformers (TA, TB, TC) and an active (uses operational amplifiers) sequence network is contained on the F148 printed circuit card in position AC. The voltage at the V_2 test jack is given by the relationship:

* V_2 test jack = $0.21 \times V_{2A} \angle 270^0$

where V_{2A} is the negative-sequence component of the input voltage referenced to phase A.

Potentiometers P1 and P2 are used to cancel small errors due to the potential source which supplies the relay.

C. Negative-sequence Current Network

The negative-sequence current network is shown on the internal connection diagram of Figure 1. The negative-sequence current network consists of three phase-to-phase current transformers (TD, TE, TF), three loading reactors (X1, X2, X3) and an active sequence network contained on the F150 card in the B position. A second active network is contained on the F149 card in position C. Two networks are used in order to include the full range of currents needed for the various negative-sequence current functions.

The voltage at the I_2 test jack is given by the relationship:

* I_2 test jack = $0.131 \times I_{2A} \angle 0^0$

where I_{2A} is the negative-sequence component of the input current referenced to phase A.

The voltage at pin 9 of the F150 card (the network output) is given by:

* Voltage at pin 9 = $0.420 \times I_{2A} \angle 0^0$

D. Negative-sequence Directional Units ($D_2(T)$, $D_2(B)$)

The input quantities to the negative-sequence-directional units are V_2 and I_2Z. The directional action is determined by the coincidence between the quantities $V_2 - I_2Z'$ and $-I_2Z$. The coincidence is measured by the $D_2(T)$ and $D_{2(B)}$ timers. The phase angle of the V_2 signal is adjustable and can be set for 0 degrees, 10 degrees, 20 degrees and 30 degrees lead. When the V_2 phase angle is set for 0 degrees, V_2 and $-I_2Z$ will be in phase if the system impedance angle is 85 degrees. The $D_2(T)$ function will produce an output for a fault in the tripping direction if negative-sequence quantities are generated. Similarly the $D_2(B)$ function will produce an output for an external fault behind the relay. The unit is designed such that with negative-sequence current applied, without negative-sequence voltage being present, the $D_2(T)$ function will operate.

E. Overcurrent Functions

There are two classes of overcurrent functions included in the SLCN51D: the unrestrained overcurrent units and the restrained overcurrent units. The unrestrained overcurrent units include: $I_2(B)$, I_2T, $I_1(B)$, $I_1(T)$, I_1T & $I_0(T)$. Each of these units consists of a filter and level detector. A bypass of the filter is provided for fast response on high current faults.

The restrained overcurrent functions include: $(I_2-K_1I_1)(T)$, $I_0-K_TI_1)(T)$, and $(I_0-K_TI_1)T$. The operation of these units will be described using the $(I_2-K_1I_1)(T)$ function. This unit will produce an output whenever the root-mean-square value of I_2 minus the root-mean-square value of K_1I_1 is greater than the preset pickup of the unit. A potentiometer is provided to adjust the K_1 factor, that is, the amount of I_1 used as restraint.

* Indicates revision

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack of cabinets with other static relays and test equipment. Immediately upon receipt of a static relay equipment it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, and metallic chips, and severe atmospheric contaiminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay unit front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

INSTALLATION TESTS

CAUTION

THE LOGIC SYSTEM SIDE OF THE D-C POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY.

NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

A. Construction

The SLCN51D relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The case is suitable for mounting on a standard 19-inch rack. The outline and mounting dimensions and the physical location of the components are shown in Figures 2 & 3 respectively.

The current and potential enter the SLCN51D on twelve-point terminal strips located on the rear of the relay case. The potential connections are made on the RA terminal strip, the current on the RB and RC terminal strip.

The basic minimum ohmic tap (T_B) setting for the $3I_0$ circuit is accomplished on the RB terminal strip on the rear of the unit. For the 1Ω tap use RC8 and RC9, for the 3Ω tap use RC8 and RC10.

The V_2, I_2 and I_0Z test jacks are located on the front of the unit. The negative-sequence voltage-network trimmer potentiometers (P1 and P2) are located on the rear of the unit.

The SLCN51D relay also contains printed circuit cards identified by a code number such as: F148, C105, D115, T133, N110 where F designates filter, C designates coincidence, D designates level detector, T designates time delay and N designates network. The printed circuit cards plug in from the front of the unit. The sockets are identified by letter designations or "addresses" (D, E, AC etc.) which appear on the guide strips in front of each socket, on the component location diagram, on the internal connection diagram, and on the printed circuit card itself. The test points (TP1, TP2 etc.), shown on the internal connection diagram, are connected to instrument test jacks on a test card in position T or AT. The jacks are numbered from top to bottom with TP1 to TP10 on the AT card and TP11 to TP20 on the T card. TP1 is connected to relay reference, TP2 is connected to -15 volt d-c and TP10 to +15 volt d-c. Output signals are measured with respect to relay reference. Logic signals are approximately +15 volt d-c for the ON or "logic one" condition, and less than one volt d-c for the OFF or "logic zero" condition. Filter card outputs are analog signals with a range of -15 volt to +15 volt. The internal connections and information on design and testing of the printed circuit cards may be found in the Printed Circuit Card Instruction Book GEK-34158.

Relay signals can be monitored with an oscilloscope, a portable high-impedance voltmeter, or the equipment-test panel meter. When time-delay cards are to be adjusted or checked, an oscilloscope which can display two traces simultaneously and which has a calibrated horizontal sweep should be used.

When the SLCN51D relay is mounted in a static relay equipment, the incoming potential and current circuits pass through test receptacles on the equipment test panel. The potential test plug is labeled PTP, the *

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* current CTP. These plugs may be replaced with type XLA test plugs which allow test currents and voltages to be supplied to the relay while maintaining a continuous path for the secondary current. Injecting the currents and voltages at this point allows all relays in the equipment to be supplied with the same current and voltage. This is particularly helpful in setting the positive-sequence-overcurrent functions because the network which supplied the input to these functions is in the associated type SLYP relay.

B. Required Tests and Adjustments

The SLCN51D relay is usually supplied from the factory mounted and wired as part of a complete static relay equipment. The necessary tests and adjustments are listed below, those marked with an asterisk must be set by the user. All steps should be performed per the procedures under DETAILED TESTING INSTRUCTIONS to insure that no shipping damage has occurred. The steps should be performed in the order shown.

1) Basic minimum ohmic tap setting*
2) Negative-sequence voltage network balance setting*
3) Sequence network calibration check
4) Negative-sequence direction unit settings

   a) voltage phase shift adjustment*
   b) offset (I_2Z) adjustment*
   c) characteristic timer setting
   d) directional action check

5) Unrestrained overcurrent level detector pickup settings*
6) Restrained overcurrent level detector pickup settings*

   a) timer setting
   b) pickup setting
   c) K factor setting

7) I_2TOC level detector settings*

   a) pickup setting
   b) time dial setting

C. Detailed Testing Instructions

1. Basic Ohmic Tap

The selection of the basic ohmic tap is discussed under CONSTRUCTION. The choice of tap setting is discussed in a separate writeup entitled OVERALL LOGIC DESCRIPTION.

2. Negative-sequence Voltage Balance Setting.

The purpose of this test is to adjust the trimmer potentiometers P1 and P2. Because these potentiometers are intended to correct small errors due to the potential source, it is necessary to set these pots with the unit connected to the system. For preliminary tests before installation, these potentiometers may be left at the factory setting.

With the connections of Figure 4, observe the waveform at the V_2 test jack with the oscilloscope. This voltage should be less than 0.3 volt peak-to-peak and consist primarily of third harmonic. Potentiometers P1 and P2 may be alternately adjusted to lower the magnitude of the signal at the V_2 test jack.

3. Sequence Network Calibration Checks

   a) Negative-sequence Voltage Network

Use the negative-sequence connections of Figure 5, apply 45 volt Ø-Ø. Use a voltmeter and check for 5.3-5.7 volt root-mean-square at the V_2 test jack.

   b) Negative-sequence Current Networks

Use the positive-sequence connections of Figure 6 to check the null of the negative-sequence current networks. Set the current in each phase for 5 amperes. Use an oscilloscope to check the voltage waveform at the I_2 test jack and at pin 9 of the B card (place B card (F150) in a card extender). This voltage should be primarily third harmonic and less than 0.2 volt peak-to-peak. Due to the accuracy of the circuit components, no adjustment is provided on these networks.

Use the negative-sequence connections of Figure 6 to check the response of the negative-sequence current networks. Set the current in each phase for 5 amperes. Use a voltmeter to measure the voltage at the I_2 test jack and at pin 9 of the B card. The voltages should be within the limits shown below.

I_2 test jack	0.6 - 0.7 volt rms
Card B Pin 9	2.0 - 2.2 volt rms

4. Negative-sequence Directional Units

a) Negative-sequence Voltage Phase Shift

Set plug W on the F148 card in the AC socket to position 0, 1, 2 or 3 depending on the desired phase shift. The phase shift for each position is shown below.

Plug W Position	Degrees of Leading Phase Shift
0	0^0
1	10^0
2	20^0
3	30^0

b) Offset (I_2Z') Adjustment

The offset reach (Z') is controlled by adjusting Plug X on the F149 card in card socket C, the W plug on the F149 card and potentiometer P1 on the F148 card in socket AC. Plug X selects the proper range of offset as shown below. P1 provides a vernier adjustment. The W plug doubles the offset when placed in the 3-Position.

Plug X Position	Offset Range Plug W in Position 1	Offset Range Plug W in Position 3
1	3.0 - 6.0Ω	6.0 - 12.0Ω
2	1.2 - 3.0Ω	
3	0.6 - 1.2Ω	
4	0.24 - 0.6Ω *	

If a non-zero offset is desired, the Y option plug on the F148 card in position AC must be set in the 1-Position. If zero offset is desired, set the Y plug to the 2-Position; no other settings are required. The following procedure is recommended to set the offset impedance:

1) Set the Y plug to the 1-Position.
Set the X plug to the position that includes the desired offset setting. Use the highest numerical tap position possible. Set Plug W in the 1-Position for all offsets less than 6Ω.

2) Set the test current of Figure 7 to 5 amperes.
Set the test voltage for 5 amperes times the offset setting in ohms. (Vtest = 5 X Z').

* 3) Adjust the phase angle for 85 degrees minus the V_2 phase shift setting (section 'a' above)

4) Connect a scope probe to Pin 8 of the F148 card in location AC.

5) Adjust P1 on the F148 card to obtain a minimum voltage at Pin 8.

Readjust the phase angle to further minimize the output. Remain within 2 degrees of the angle found in Step 3.

If output is greater than 2 volts peak-to-peak, repeat Steps 5 and 6.

c) D_2 (T)/D_2(B) Characteristic Timer Setting

The timers used for $D_2(T)$, $D_2(B)$, $(I_2\text{-}KI_1)(T)$, $(I_0\text{-}KI_1)(T)$ and $(I_0\text{-}KI_1)T$ are integrating characteristic timers. These timers are shown on the overall logic as T_1 T_2/T_3 where T_1 is the input on a step d-c input, T_2 is the pulse width which will cause the timer to pick up with one pulse applied per half cycle, and T3 is

* Indicates revision

the dropout time. T_2 is always less than T_1, thus the timer integrates when a chain of pulses is applied. The two pickup modes are depicted in Figure 8.

It should be noted that the characteristic timers have been set at the factory. The settings may be verified by the following procedure. The d-c pickup time(T_1) and the dropout time (T3) may be checked using a d-c input and a normally closed contact as shown in Figure 9. Opening the normally closed contact causes the timer output to step to 15 volt d-c after the pickup delay of the timer. To increase the pickup delay turn the upper potentiometer (P1) on the card clockwise. Closing the contact causes the timer output to drop out after the reset-delay setting of the timer. To increase the reset time, turn potentiometer P2 clockwise. P2 is the middle potentiometer on the T133 card and the lower on the T129 card. When performing these tests the card which normally supplies the input to the timer should be removed as shown in the following table.

Timer Under Test	Remove Card
$D_2(T)$	AE
**$D_2(B)$	AE
$(I_2-K_1 I_1)$ (T)	G
$(I_0 -KI_1)$ (T)	J
$(I_0 -K_T I_1)$ T	L

**Connect AK4 to reference since a fast reset input will prevent the timer from operating.

To set the integration on the T133 type timer, it is necessary to supply the timer card with an input consisting of a series of pulses. This can be accomplished by adjusting the input currents, voltages or the phase angle between them to achieve the desired width pulses. Potentiometer P3 (lower potentiometer on the T133 cards) may now be adjusted to cause the timer to pickup, turning P3 clockwise increases the integration (picks up on smaller blocks).

To set the integration on the $D_2(T)$ characteristic timer set the current and the voltage for the value determined in Step 2 of Section "b"; use the test connections of Figure 7. Adjust the phase angle until the pulses at TP3 (timer input) reach the desired width. Adjust P3 to just obtain pickup.

d) Direction Action Check

1) Use the test circuit of Figure 7. Set the current for one ampere and the voltage for twice that used in Step 2 of Section "b".

* 2) Set the phase shifter for 265 degrees minus the V_2 phase shift setting (Section "a"). Check that $D_2(T)$ operates and $D_2(B)$ does not.

* 3) Adjust phase shifter 180 degrees from the setting of Step 2. Check that $D_2(B)$ operates and $D_2(T)$ does not.

5. Unrestrained Overcurrent Level Detectors

a) Pickup Setting

The pickup level of the $I_0(T)$, $I_2(B)$, I_2T, $I_1(B)$, $I_1(T)$ and I_1T functions may all be set using the test circuit of Figure 10. The pickup level of the unrestrained overcurrent functions is controlled by the X
* option plug and potentiometer P20 (upper potentiometer) on the level detector card under test. The X option
* plug selects the proper pickup current range and P20 provides a vernier adjustment. The pickup range for each X plug position is shown in the following table. Where a setting may be obtained in two plug positions the highest number tap should be used.

FUNCTION RANGE	CARD LOCATION	OUTPUT TEST POINT	OPTION X TAP	RANGE	CURRENT
* I_1 (B) 0.5-4.0	P	TP17	1 2 3 4	0.5 to 1.0 1.0 to 1.6 1.6 to 3.25 3.25 to 4.0	Ampere I_1

* Indicates revision

FUNCTION RANGE	CARD LOCATION	OUTPUT TEST POINT	OPTION X TAP	RANGE	CURRENT	
I_1 (T) 1.0-8.0	R	TP16	1 2 3 4	1.0 to 1.5 1.5 to 4.0 4.0 to 7.25 7.25 to 8.00	Ampere I_1	*
I_1T 4.0-32	S	TP19	1 2 3 4	2.0 to 4.0 4.0 to 10.0 10.0 to 20.0 20.0 to 50.0	Ampere I_1	
I_2 (B) 0.2-0.6	AR	TP15	1 2 3	0.2 to 0.4 0.4 to 1.0	Ampere I_2	
I_2T 2.0-16	AS	TP18	1 2 3 4	1.0 to 2.0 2.0 to 5.0 5.0 to 10.0 10.0 to 25.0	Ampere I_2	
I_0 (T) ($3I_0$) 0.3-2.4	AP	TP14	1 2 3 4	0.3 to 0.6 0.6 to 1.25 1.25 to 2.00 2.00 to 2.4	Ampere $3I_0$	*

The following procedure is recommended:

1) Set the X option plug to the desired tap per the table.

2) Use the test connections of Figure 10. Set the test current (Itest) to the desired level. Note that Itest = $3I_1 = 3I_2 = 3I_0$. If the setting is specified in terms of positive or negative sequence current, the test current must be three times the specified setting. If the setting is specified in terms of $3I_0$ the test current must equal the setting.

3) Observe the output test point with an oscilloscope and adjust P20 on the card under test until the output just steps to +15 volt d-c. Turning the potentiometer clockwise increases the pickup setting of the unit. *

b) Dropout Timer Setting

The overcurrent function drop-out timers are factory set. The following procedure is recommended to check or reset the drop-out time.

1) Use the test connections of Figure 10. Set the test current to the pickup value of the card under test.

2) Connect the test circuit of Figure 11. Closing contact A causes the input to go to zero. Contact B triggers the scope, and the dropout time may be observed.

c) Optional G4 function

When the G4 function is included, a D114 level detector card is supplied in card Position J with a J101 jumper card (Pin 3 jumpered to Pin 8) in card position K. The pickup can be set using the test circuit of Figure 10. The following procedure is recommended.

1) Adjust the current to the desired level

2) Adjust P1 on the D114 card in Position J until the signal at TP11 just picks up.

* Indicates revision

The G4 function has a non-adjustable drop-out time of 11 milliseconds which may be checked using the test circuit of Figure 9. Refer to the CHARACTERISTIC TIMER SETTING section for the procedure.

6. Restrained Overcurrent Level Detectors

a) Characteristic Timer Settings

The d-c step pickup time and the drop-out time may be checked using the d-c switch method outlined in the negative-sequence directional unit section. The integration on the T133 timers may be set using the test circuit of Figure 10. The input current should be set such that the blocks in the timer are 4.16 milliseconds wide. An alternative method is to replace the $D_2(T)$ timer (AH position) with the level detector timer and use the procedure outlined in the negative-sequence directional unit section.

b) Pickup Setting

The pickup current level setting of the restrained overcurrent functions $(I_2-K_1I_1)$ (T), $I_0-KI_1)(T)$, and $(I_0-K_1I_1)$ (T) may be set using the test connections of Figure 10. The following procedure is recommended.

1) Place the level detector card under test (G, J or L) in a card extender and jumper Pin 6 (restraint input) to reference. This allows the pickup to be set with no restraint involved.

2) Set the test current to the desired level. Note that Itest = $3I_2 = 3I_0$. If the setting is specified in terms of negative-sequence current, the test current must be three times the specified setting. If the setting is specified in terms of $3I_0$ current, the test current must equal the specified setting.

3) Adjust P2 on the card under test (G, J or L) until the function just picks up. Turning P2 clockwise increases the pickup level. Observe the output at the test point following the characteristic timer (TP8, TP11, or TP13).

c) Restraint Factor (K) Setting

The restraint factor (K) setting may also be accomplished using the test circuit of Figure 10. Pin 6 of the card under test must not be jumpered to reference for this test. The following procedure is recommended.

1) Set the current to the level given by the following expression:

$$I_{test} = \frac{I_{test\ p.u.}}{1 - K}$$

* Where: I_{test} is the necessary current to set K

$I_{test\ p.u.}$ is the pickup test current used in section b

K is the required restraint factor

ii) Adjust potentiometer P1 on the card under test (G, J or L) until the output just picks up. Turning P1 clockwise increases the restraint factor. Observe the output at the test point following the associated characteristic timer (TP8, TP11 or TP13).

7. I_2TOC Time Overcurrent Level Detector

a) Pickup Setting

The pickup level of the I_2TOC function may be set using the test circuit of Figure 10. The pickup level is controlled by the X option plug and potentiometer P1 located on the D124 card in position AS. The X option plug selects the proper pickup current range and P1 provides a vernier adjustment. The pickup range for each X plug is shown in the following table. Where a setting may be obtained in two plug positions, the higher number tap should be used.

Option X Tap	Range (Ampere I_2)
1	0.2 - .4
2	0.4 - 1.1
3	1.1 - 2.25
4	2.25 - 3.0

* Indicates revision

The following procedure is recommended:

1) Set the X option plug to the desired tap per the table.

2) Use the test connections of Figure 10. Set the test current (Itest) to the desired pickup level. Note that Itest = $3I_2$. If the test setting is specified in terms of negative sequence amperes (I_2), the test current must be three times the specified setting.

* 3) Observe the output at TP18 and adjust P1 on the D124 card until the output just steps to +15 volt d-c. Turning the potentiometer clockwise increases the pickup setting, counterclockwise decreases the setting. Due to the time delay in the circuit it is necessary to wait 60 seconds after adjusting the potentiometer to determine if the function has picked up. Pickup may also be monitored at pin 5 of the D124 card (position AS). Pickup occurs when the voltage at pin 5 drops from +15VDC to -15VDC.

b) Time Overcurrent Setting

There are two time-dial adjustments on this function: a time dial and a time-dial vernier. The time dial is a rotary switch mounted on the D124 card. The numbered positions on this switch (1 through 10) correspond to the time-dial numbers on the time-current curves of Figure 12. The rotary switch has a detent mechanism which engages as the time-dial switch is turned to the desired setting. Care should be taken that the number of the desired time-dial setting lines up with the marker dot at the base of the switch.

The time-dial vernier is potentiometer P2 on the D124 card. This vernier may be used to set the function between the integer time-dial curves. The vernier increases the setting of the time-dial switch. The time-dial vernier (P2) must be set fully counterclockwise for the I_2TOC operating characteristic to be one of the integer time-dial time-current curves of Figure 12; otherwise the actual time-current curve will be between two of the published curves.

The following procedure is recommended for checking the time-overcurrent feature.

1) Set pickup as described previously.

2) Set time-dial switch to the desired time-dial setting. Adjust the time-dial vernier (P2) fully counterclockwise.

3) Use the test circuit of Figure 13. Set current for five times pickup. Close switch to suddenly apply current and check pickup time for several trials. The average time should be with 0.1 second or 7 percent of the published curve, whichever is greater.

PERIODIC CHECKS AND ROUTINE MAINTENANCE

1. Periodic Tests

All of the functions included in the SLCN51D relay may be checked at periodic intervals using the procedures described in Installation Tests. Cable connections between the SLCN51D relay and the associated type SLA logic unit may be checked by observing the test points in the SLA relay.

The following checks should be made during periodic tests:

a) Directional-unit offset check
b) Directional action check
c) Overcurrent-pickup level check

2. Trouble Shooting

In any trouble shooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it would be possible to quickly isolate the trouble.

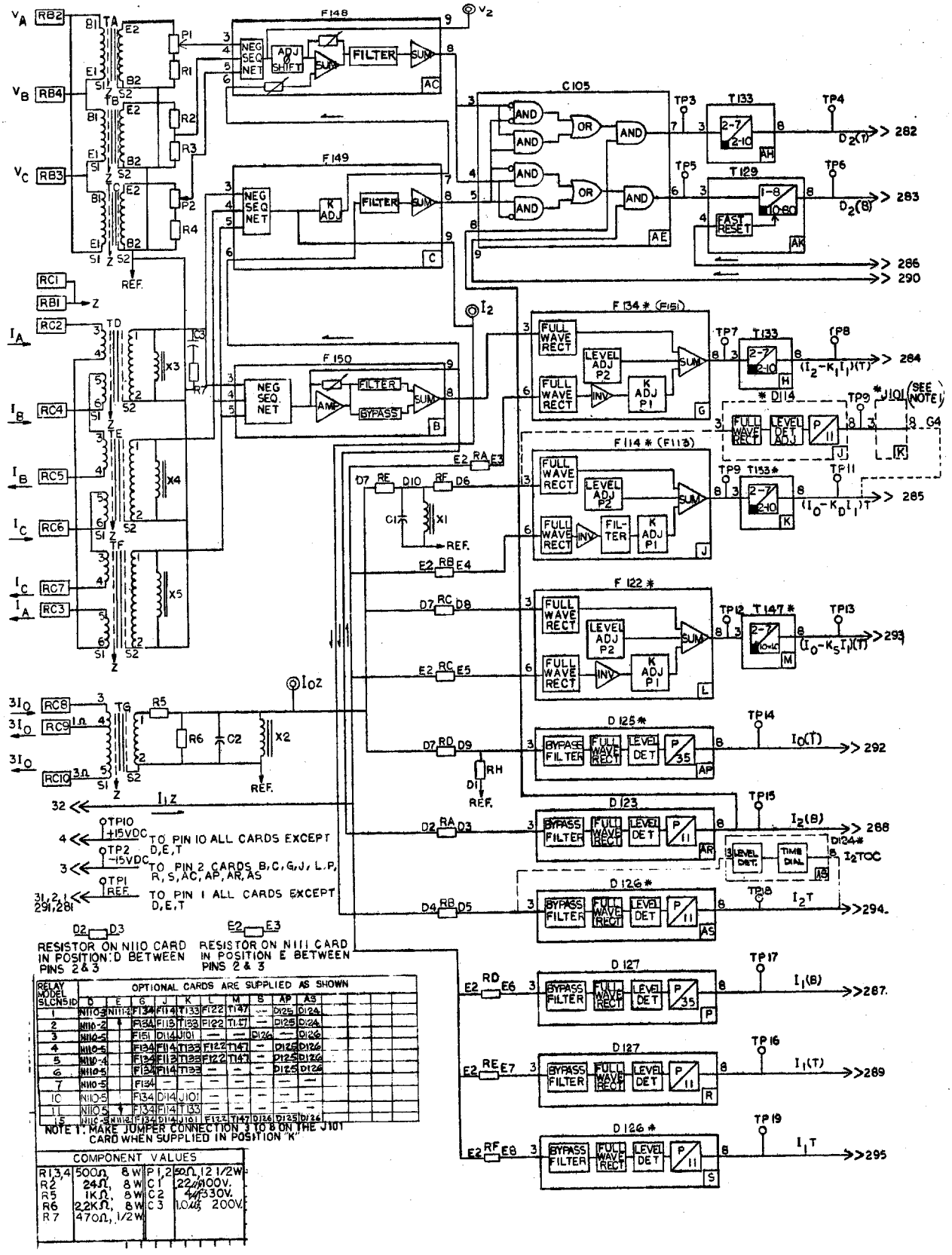
A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed trouble shooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

* Indicates revision

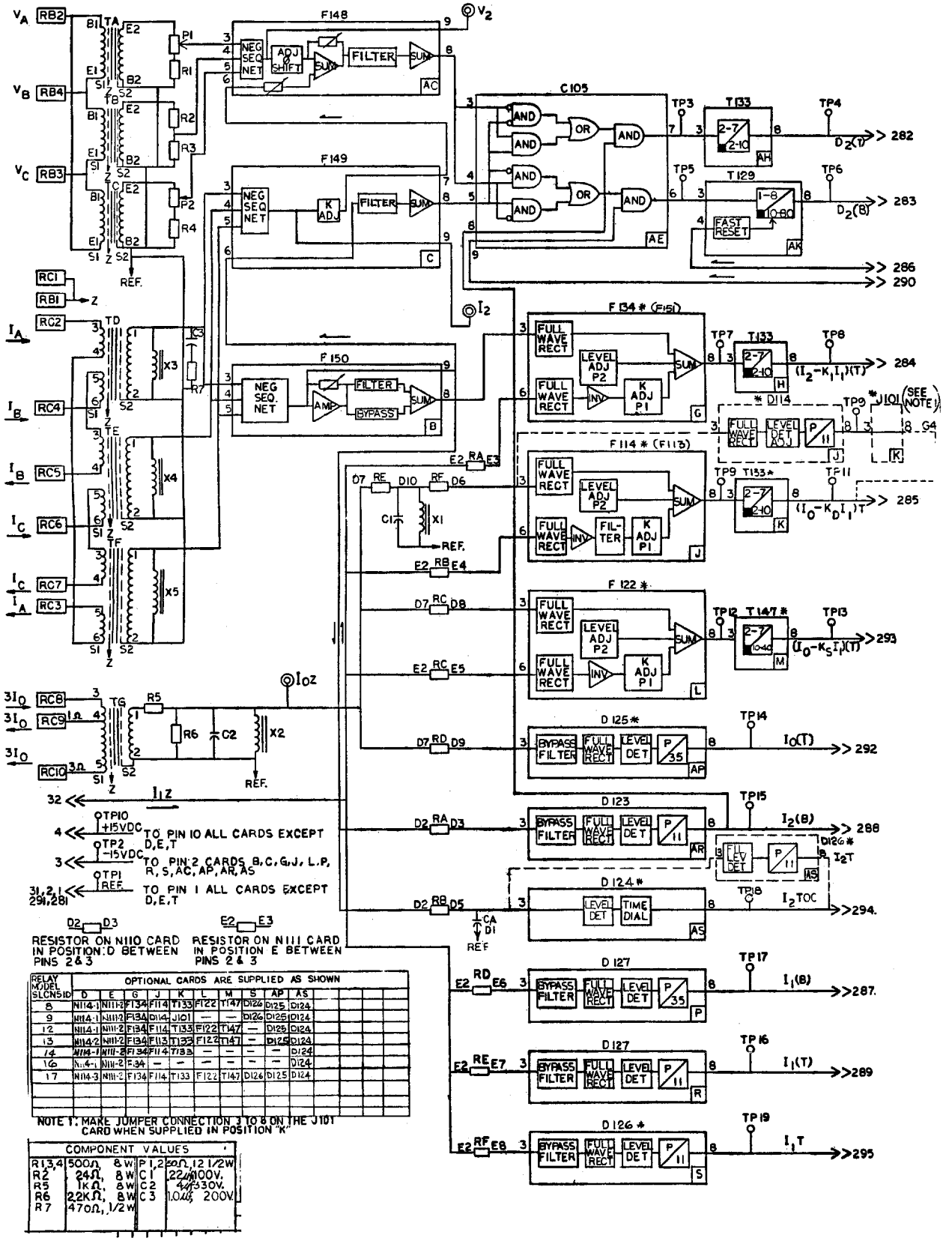
3. Spare Parts

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of a least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLCN51D relay are included in the card book GEK-34158; the card types are shown on the component location diagram, Figure 3.



* Fig. 1A (0171C7857-8) Internal Connections Diagram for the SLCN51D Relay without I_2 TOC

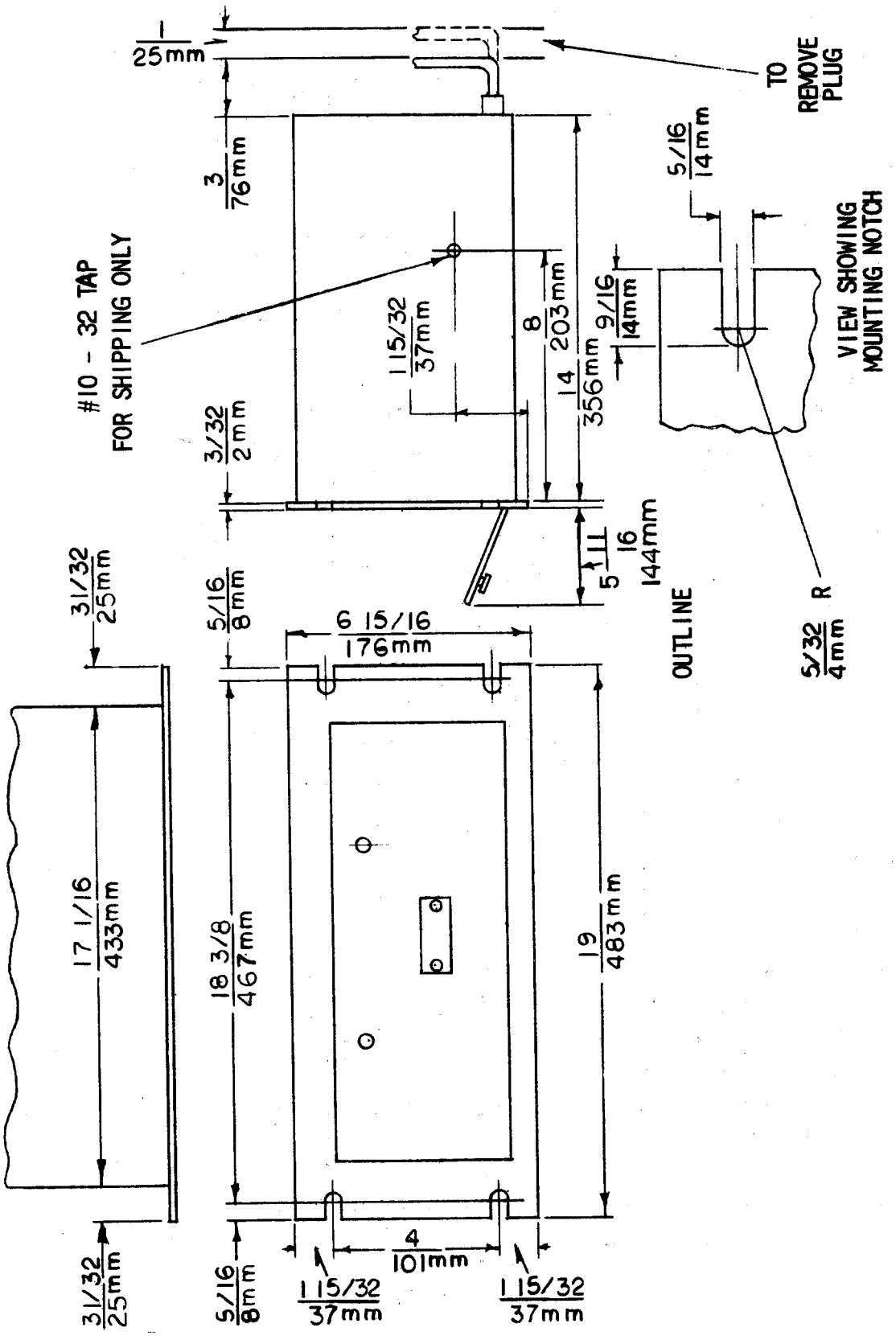
* Indicates revision



RELAY MODEL SLCN51D	OPTIONAL CARDS ARE SUPPLIED AS SHOWN									
	D	E	G	J	K	L	M	S	AP	AS
8	N114-1	N111-2	F134	F114	T133	F122	T147	D126	D125	D124
9	N114-1	N111-2	F134	D114	J101	—	—	D126	D125	D124
12	N114-1	N111-2	F134	F114	T133	F122	T147	—	D125	D124
13	N114-2	N111-2	F134	F113	T133	F122	T147	—	D125	D124
14	N114-1	N111-3	F134	F114	T133	—	—	—	—	D124
16	N114-1	N111-2	F134	—	—	—	—	—	—	D124
17	N114-3	N111-2	F134	F114	T133	F122	T147	D126	D125	D124

* Fig. 1B (0152C8471-2) Internal Connections Diagram for the SLCN51D Relay with I_2 TOC

* Indicates revision



* Fig. 2 (0227A2037-1) Outline and Mounting Dimensions for the SLCN51D Relay

* Indicates revision

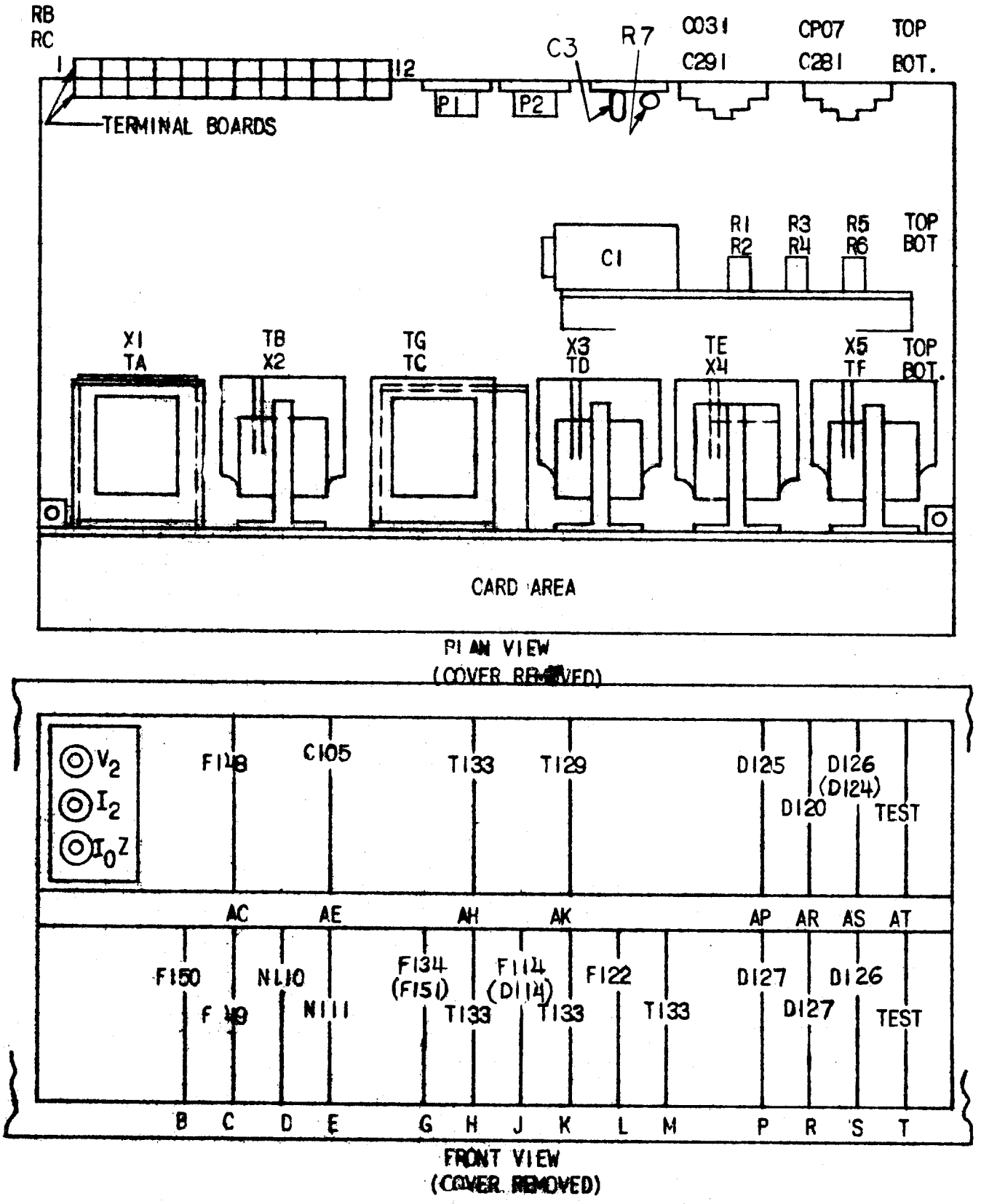


Fig. 3 (0257A8777-1) Component Location Diagram for the SLCN51D Relay

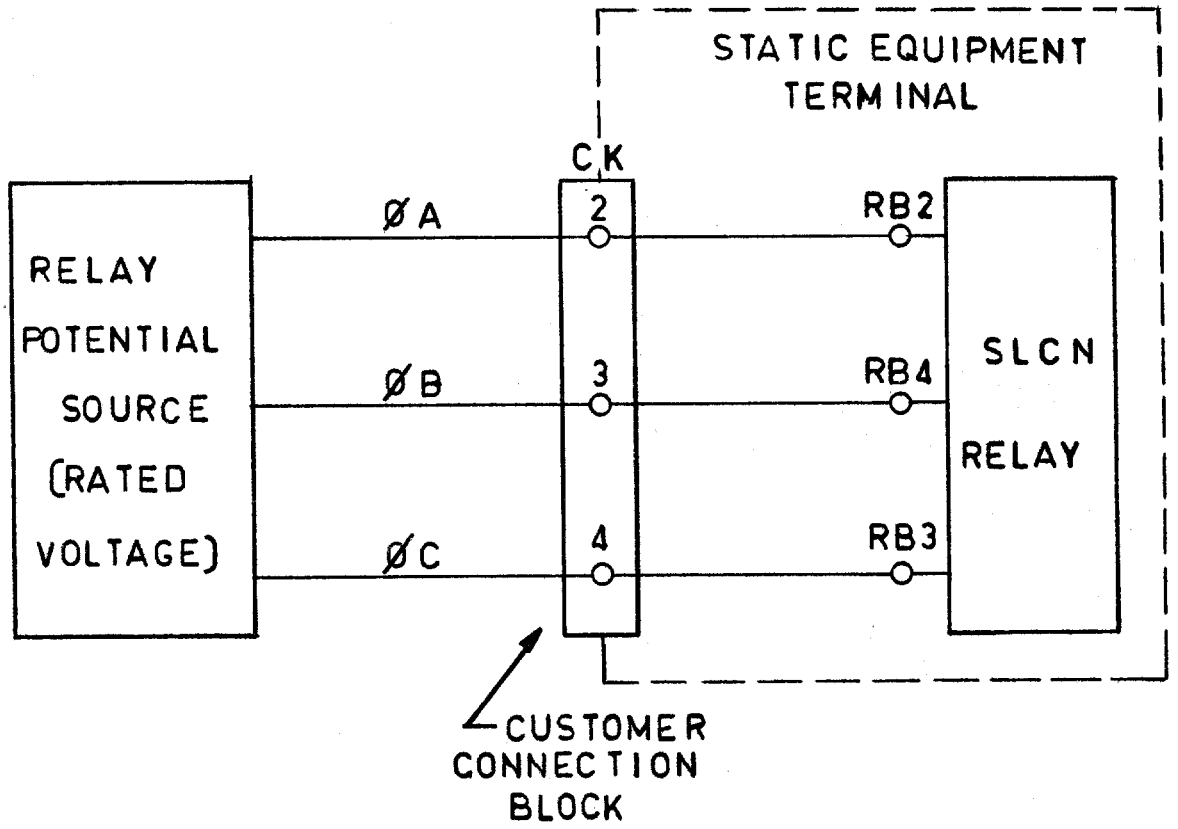


Fig. 4 (0257A9619-0) Test Circuit for Negative-sequence Voltage Network Balance Check

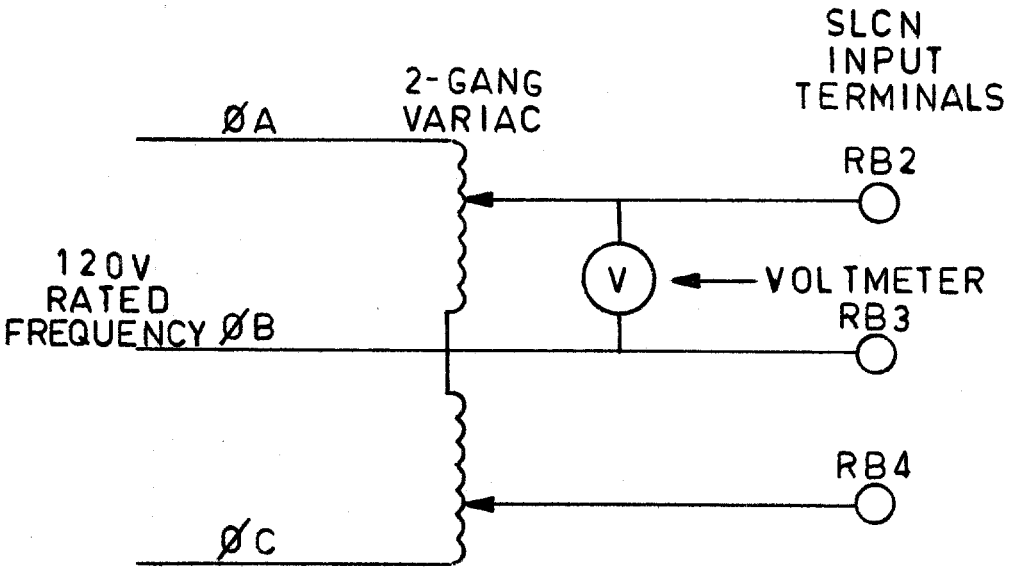


Fig. 5 (0257A9620-0) Negative-sequence Voltage Network Test Circuit

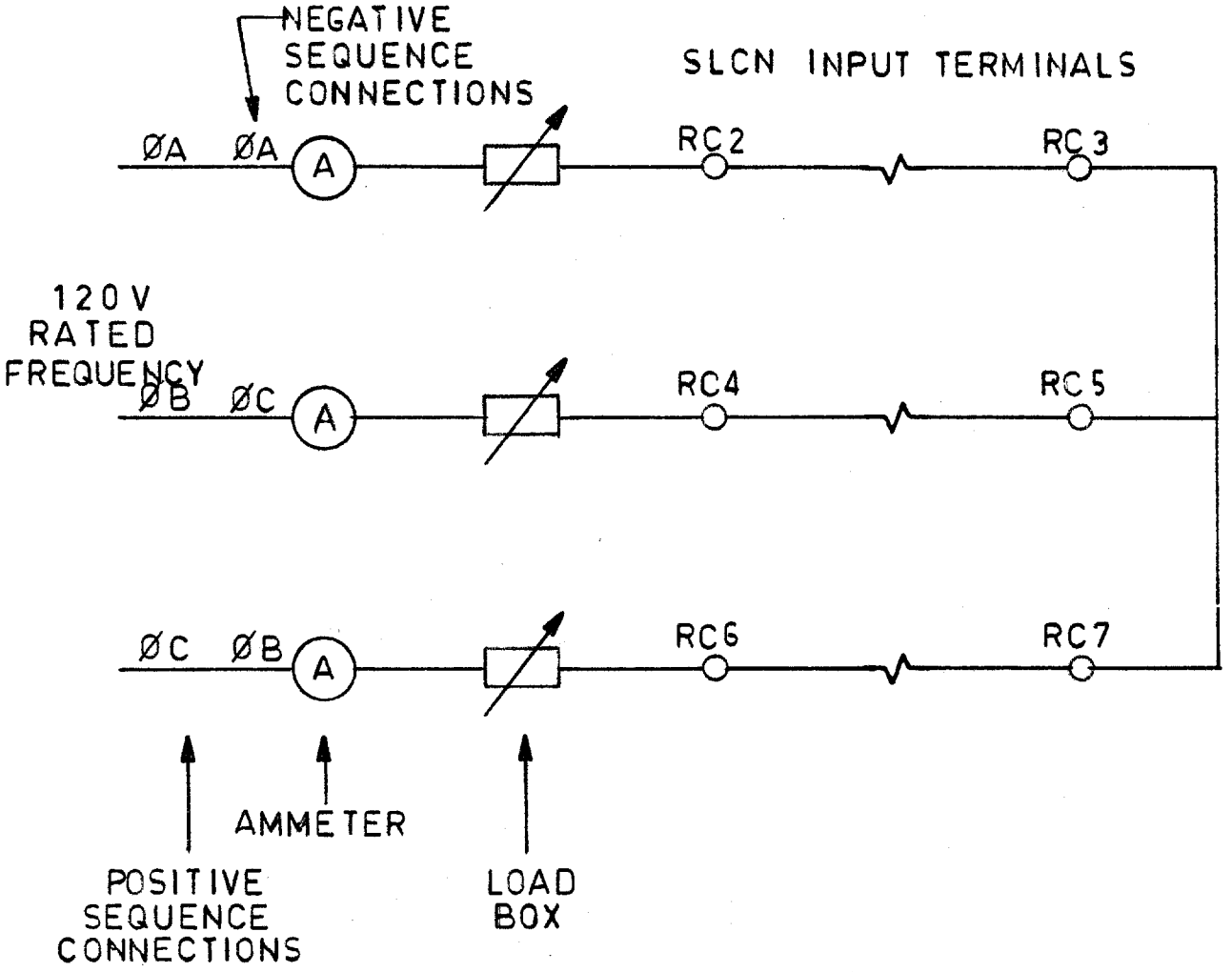


Fig. 6 (0257A9621-0) Negative-sequence Current Network Test Circuit

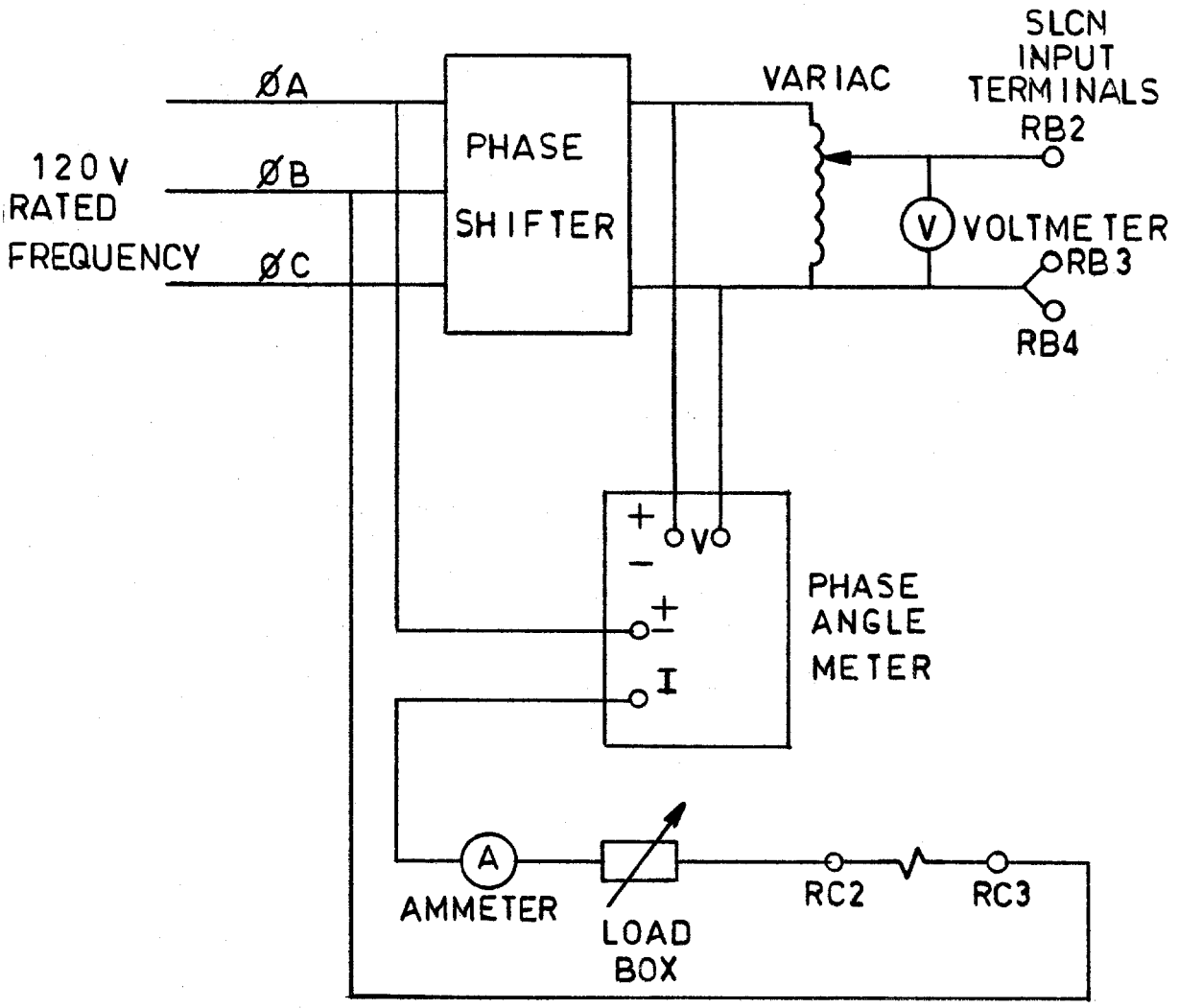


Fig. 7 (0257A9623-0) Negative-sequence Directional Unit Test Circuit

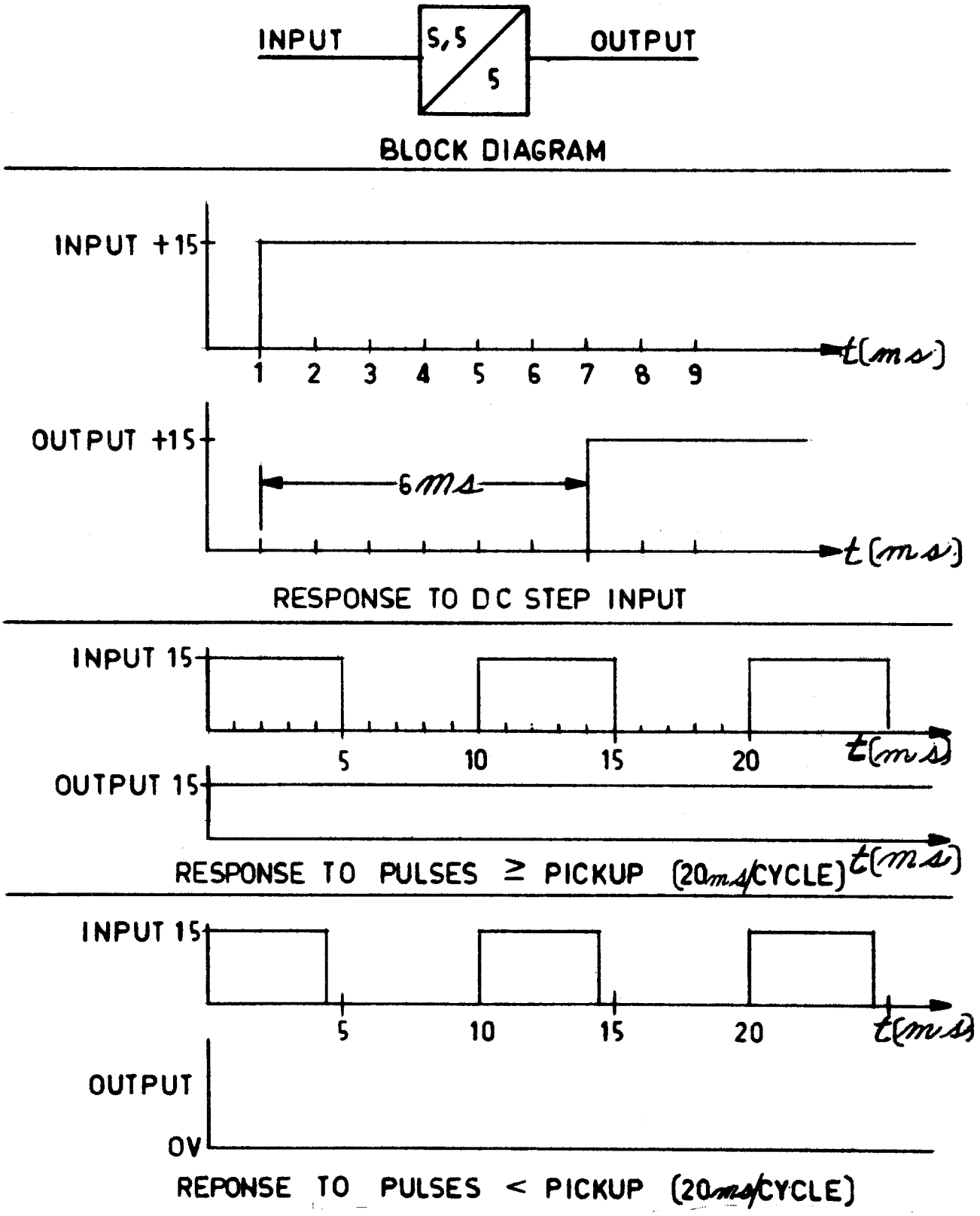
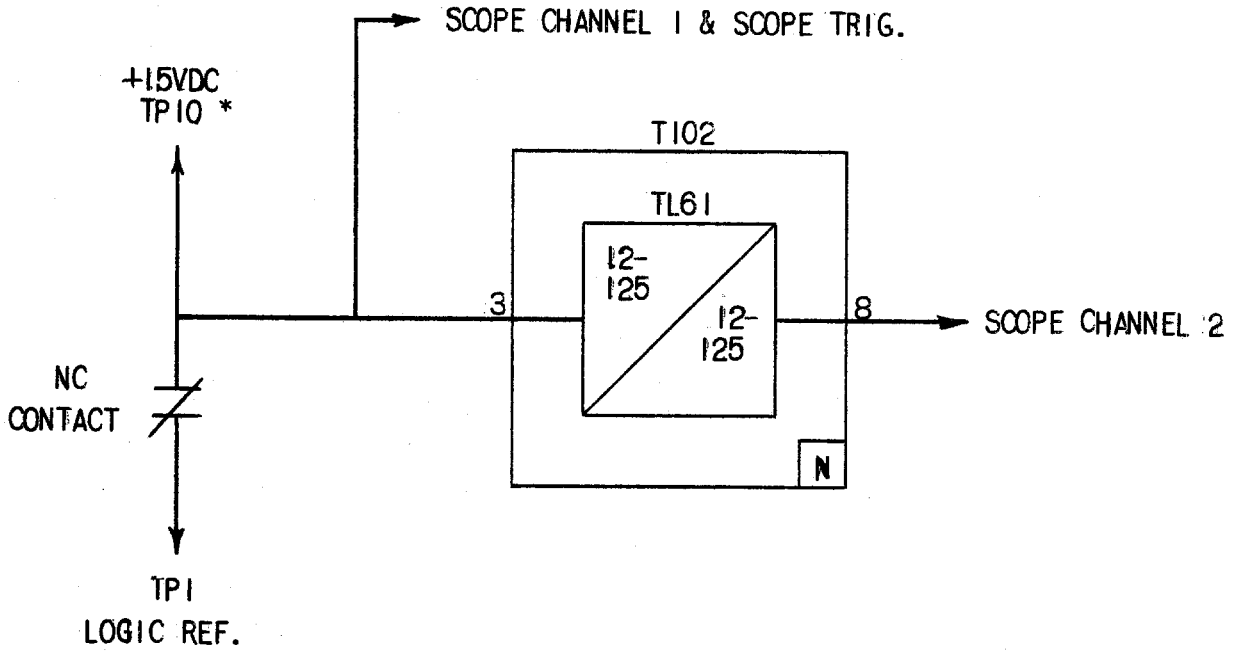


Fig. 8 (0257A9624-0) Integrating Characteristic Timer Pickup Waveforms



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 9 (0246A7987-0) Timer Test Circuit

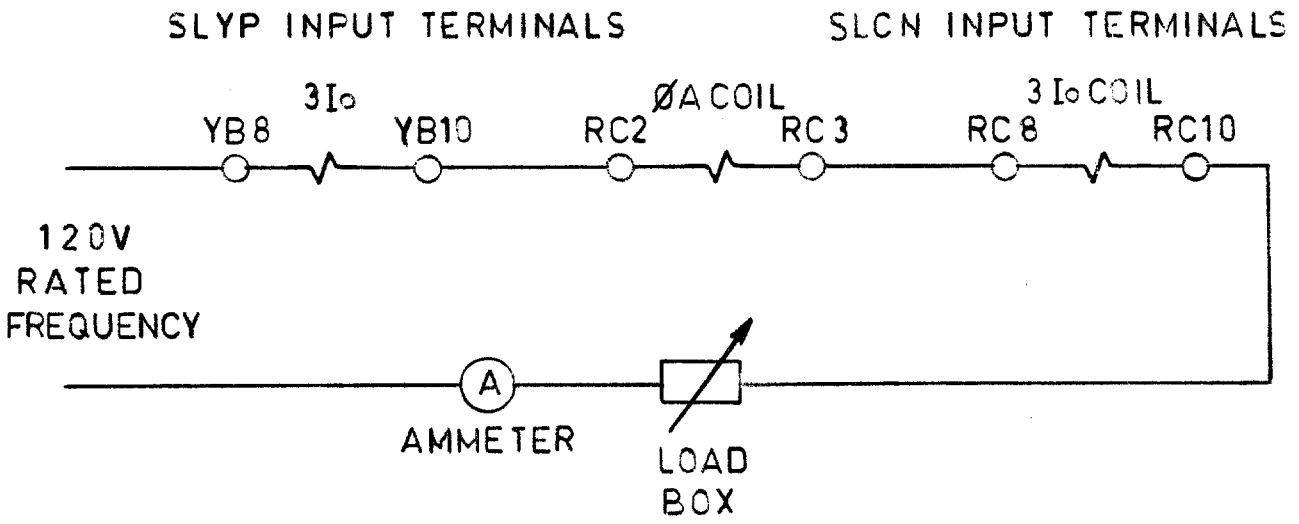


Fig. 10 (0257A9622-0) Overcurrent Level Detector Test Circuit

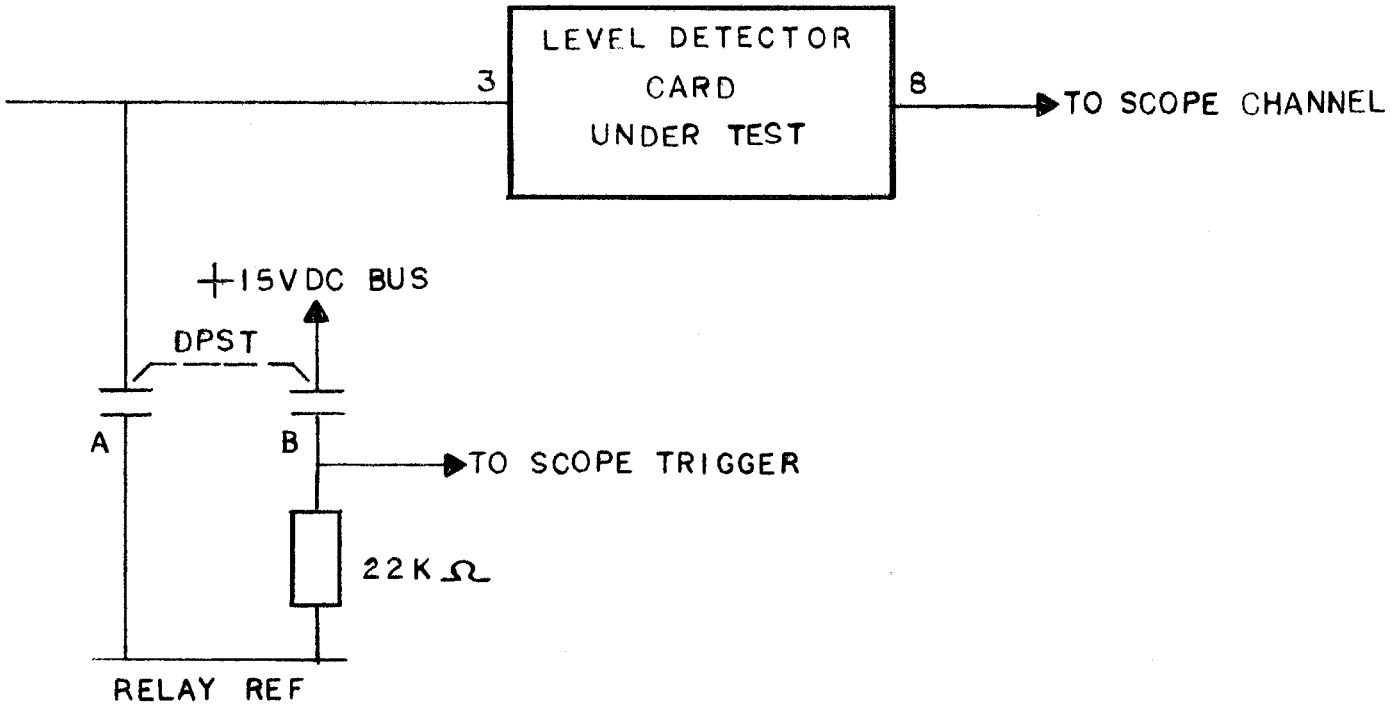


Fig. 11 (0257A8735-0) Overcurrent Level Detector Drop-out Timer Test Circuit

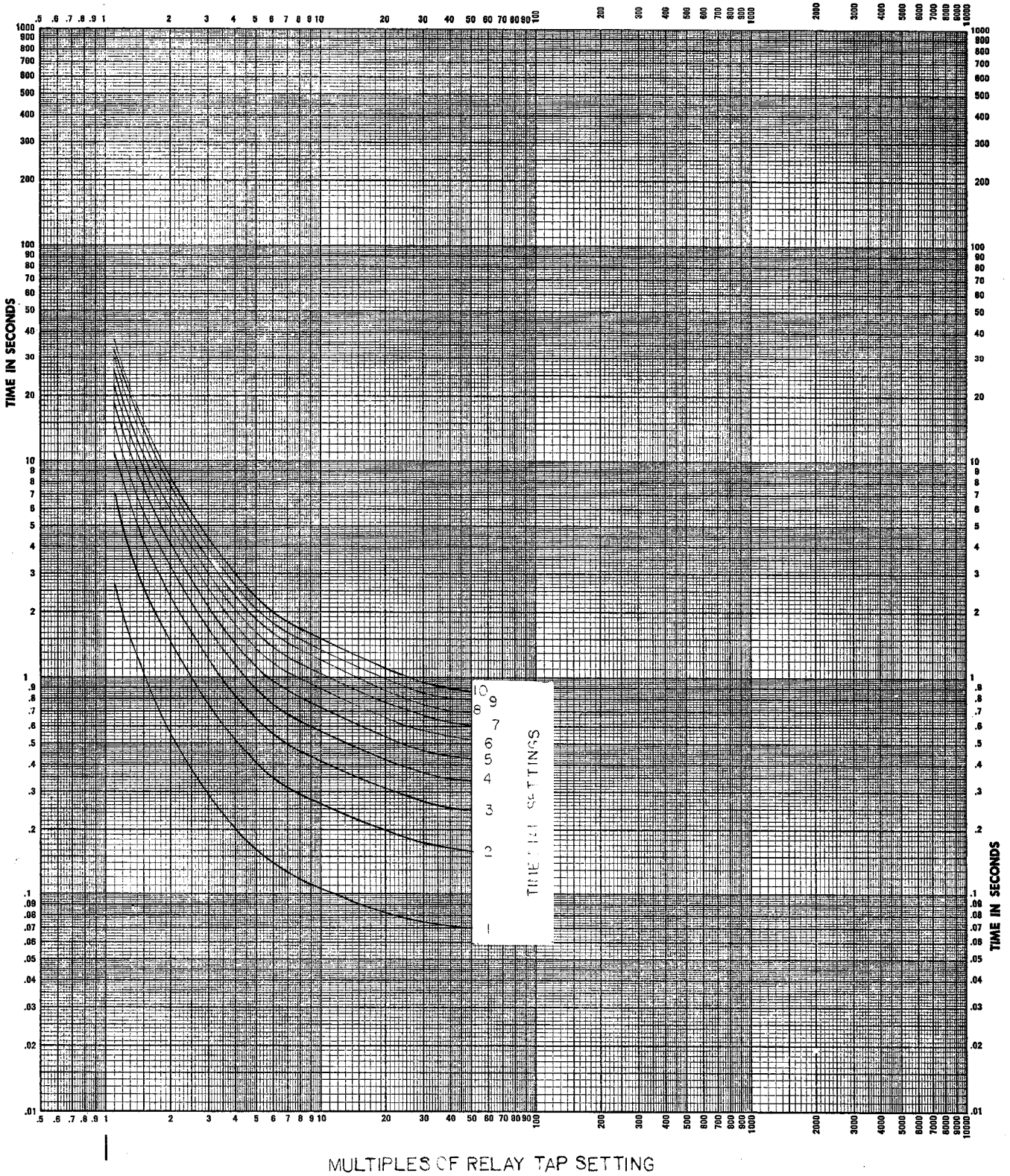


Fig. 12 (0183B7888-0) I_2TOC Time-current Curves

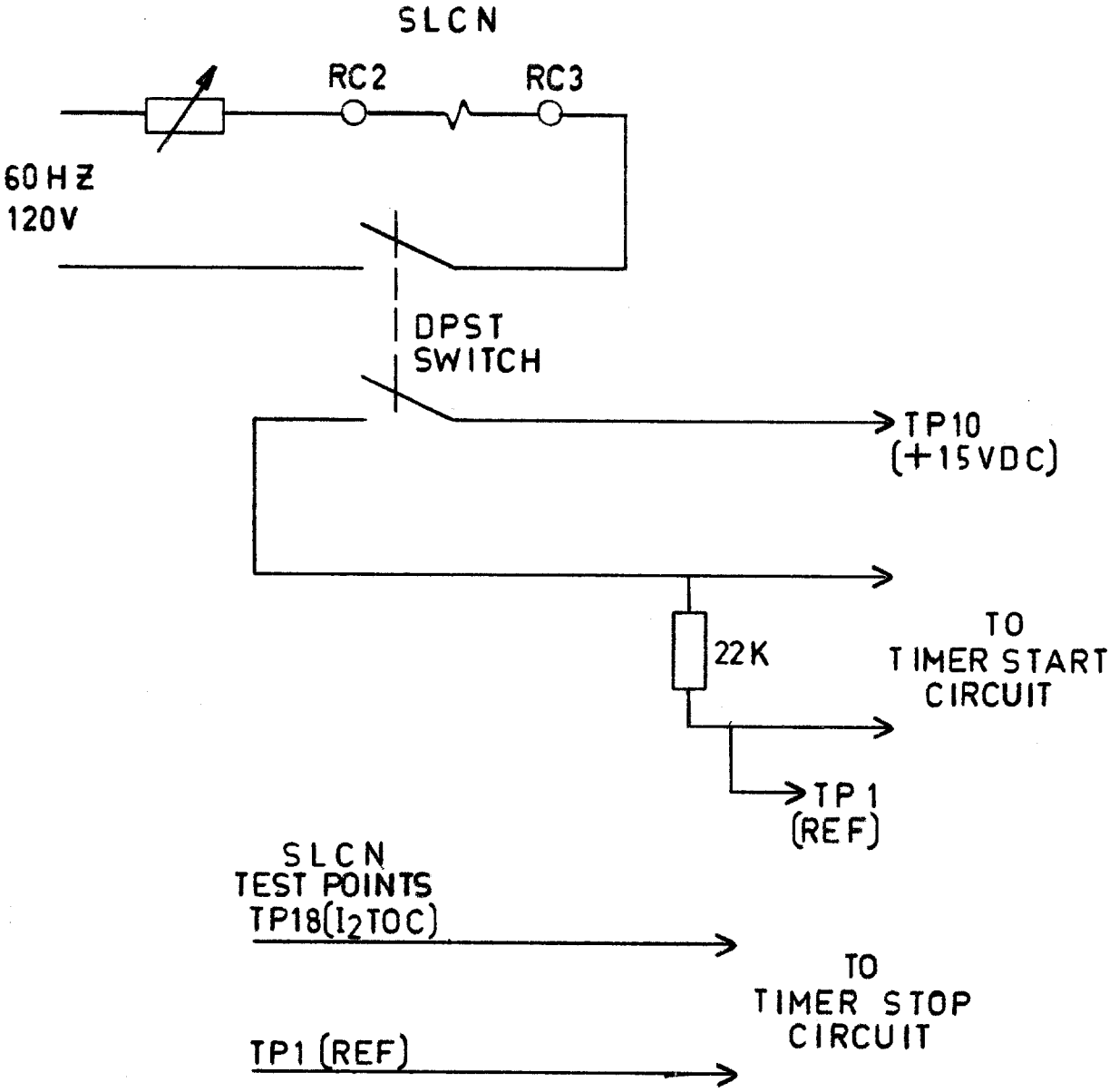


Fig. 13 (0257A8798-0) Time Overcurrent Test Circuit